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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Leonard Forbes et al.

Title: CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED SEMICONDUCTOR SURFACES AND METHODS FOR FORMING THE SAME

Attorney Docket No.: 303.389US2

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
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We are transmitting herewith the following attached items and information (as indicated with an "X"):

X **DIVISIONAL** of prior Patent Application No. 09/010,729 (under 37 CFR § 1.53(b)) comprising:
- X Specification (19 pgs, including claims numbered 1 through 30 and a 1 page Abstract).
- X Formal Drawing(s) (5 sheets).
- X Copy of signed Combined Declaration and Power of Attorney (9 pgs) from prior application.
- X Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
- X Check in the amount of $760.00 to pay the filing fee.

X Prior application is assigned of record to Micron Technology, Inc..

X Information Disclosure Statement (1 pgs), Form 1449 (12 pgs). References NOT enclosed, cited in prior application.

X Preliminary Amendment (1 pgs).

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TOTAL CLAIMS	14 - 20 =	0	x 18 =	$0.00
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.389US2
Title:	CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED SEMICONDUCTOR SURFACES AND METHODS FOR FORMING THE SAME	

PRELIMINARY AMENDMENT

Box Patent Application
Assistant Commissioner for Patents
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Before taking up the above-identified application for examination, please enter the following amendments.

IN THE SPECIFICATION

In the first line after the title please insert the following, --This application is a Divisional of U.S. Application No. 09/010,729, filed January 22, 1998.--

IN THE CLAIMS

Please cancel claims 1-16 without prejudice or disclaimer, claims 17-30 are therefore now pending in this application.

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Respectfully submitted,

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Circuits with a Trench Capacitor Having Micro-Roughened Semiconductor Surfaces and Methods for Forming the Same

Technical Field of the Invention

The present invention relates generally to the field of integrated circuits and, in particular, to circuits with a trench capacitor having micro-roughened semiconductor surfaces and methods for forming the same.

Background of the Invention

Electronic systems, such as microprocessor based computers, typically operate on data that is stored in electronic form in a memory device. The memory device stores the data at specified voltage levels in an array of cells. Conventionally, the voltage levels represent that the data is either a logical "1" or a logical "0." In dynamic random access memory (DRAM) devices, for example, the cells store the data as a charge on a capacitor. When the data is read from the memory device, sense amplifiers detect the level of charge stored on a particular capacitor so as to produce a logical "1" or a logical "0" output based on the stored charge.

As the size of memory devices decreases, the capacitor in each cell covers a smaller surface area or footprint on the substrate, chip or wafer. If the structure of the capacitor is left unchanged, these smaller capacitors cannot store as much charge because the storage capacity of a typical capacitor is proportional to the size of its storage electrodes. Unfortunately, at some point, the capacitors become too small to store sufficient charge and sense amplifiers in the memory device are unable to differentiate between charge due to noise and the charge due to data stored in the cell. This can lead to errors in the output of a memory device making the memory device useless in the electronic system.

Conventionally, memory manufacturers have used one of two types of capacitors in DRAM devices. First, many manufacturers use "stacked" capacitors to store data for the memory cell. Stacked capacitors are typically formed from polysilicon and are positioned above the conventional working surface of the

semiconductor chip or wafer on which the memory device is formed. A contact couples the capacitor to a transistor in the memory cell. Some manufacturers use "trench" capacitors instead of stacked capacitors. Trench capacitors are typically formed in a trench in the semiconductor wafer or chip. The trench is filled with polysilicon that acts as one plate of the capacitor. In this case, the semiconductor wafer or chip acts as the second plate of the capacitor.

Designers have experimented with various configurations of capacitors, both stacked and trench, to maintain the capacitance as the footprint available for the capacitor decreases. In the area of stacked capacitors, designers have used texturization, stacked V-shaped plates and other shaped plates to increase the surface area of the plates without increasing the footprint of the capacitor. For example, designers have developed techniques to produce hemispherical grains on the surface of one polysilicon plate of the stacked capacitor. This roughly doubles the storage capacity of the capacitor. Researchers have also described techniques for further increasing the surface area of the polysilicon plate, and thus the storage capacity of the capacitor, by using phosphoric acid to create pores in the polysilicon plate. *See*, Watanabe, *A Novel Stacked Capacitor with Porous-Si Electrodes for High Density DRAMs,* Symposium on VLSI Technology, pp. 17-18, 1993. With this technique, it is claimed that a 3.4 times increase in capacitance can be achieved.

One problem with the use of stacked capacitors is their positioning above the surface of the substrate. This positioning can interfere with the proper functioning of the equipment used to fabricate other parts of a larger circuit.

Conventionally, as the footprint available for trench capacitors has decreased, the manufacturers have used deeper trenches to maintain sufficient storage capacity of the trench capacitor. IBM has developed another technique in an attempt to maintain sufficient storage capacity as the footprint of the trench capacitor decreases. This technique uses an anodic etch to create pores in the single crystalline silicon in the trench of the trench capacitor. *See*, U.S. Patent No. 5,508,542 (the '542 Patent). One problem with this technique is the lack of control over the distribution of the pores in

the surface of the single crystalline silicon. Thus, the '542 Patent does not provide a technique that can be used reliably for large scale production of memory devices.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a realizable trench capacitor with increased surface area compared to prior art capacitors for use in high-density circuits such as dynamic random access memories.

Summary of the Invention

The above mentioned problems with integrated circuits and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A trench capacitor with increased surface area is described which is formed by depositing a layer of polysilicon in a trench in a semiconductor substrate and etching the polysilicon to produce a porous surface for the trench capacitor.

In particular, an illustrative embodiment of the present invention includes a method for forming a trench capacitor. The method includes forming a trench in a semiconductor substrate. A conformal layer of semiconductor material is deposited in the trench. The surface of the conformal layer of semiconductor material is roughened. An insulator layer is formed outwardly from the roughened, conformal layer of semiconductor material. A polycrystalline semiconductor plate is formed outwardly from the insulator layer in the trench.

In another embodiment, a method for forming a memory cell with a trench capacitor is provided. The method includes forming a transistor including first and second source/drain regions, a body region and a gate in a layer of semiconductor material on a substrate. Further, a trench is formed in the layer of semiconductor material and a conformal layer of semiconductor material is formed in the trench. The surface of the conformal layer of semiconductor material is roughened and an insulator layer is formed outwardly from the roughened, conformal layer of semiconductor

material. A polycrystalline semiconductor plate is formed outwardly from the insulator layer in the trench such that the polycrystalline semiconductor plate forms one of the plates of the trench capacitor. The trench capacitor is coupled to one of the first source/drain regions of the transistor.

In another embodiment, a memory cell is provided. The memory cell includes a lateral transistor formed in a layer of semiconductor material outwardly from a substrate. The transistor includes a first source/drain region, a body region and a second source/drain region. A trench capacitor is formed in a trench and coupled to the first source/drain region. The trench capacitor includes a polycrystalline semiconductor plate formed in the trench that is coupled to the first source/drain region. The trench capacitor also includes a second plate formed by the substrate with a surface of the substrate in the trench roughened by etching a polycrystalline semiconductor material on the surface of the substrate. The trench capacitor also includes an insulator layer that separates the polycrystalline semiconductor plate from the roughened surface of the substrate.

In another embodiment, a memory cell is provided. The memory cell includes a vertical transistor that is formed outwardly from a substrate. The transistor includes a first source/drain region, a body region and a second source/drain region that are vertically aligned. A surface of the first source/drain region is roughened by etching a polycrystalline semiconductor material on a surface of the first source/drain region. A trench capacitor is also included. The trench capacitor includes a plate that is formed in a trench that surrounds the roughened surface of the first source/drain region of the transistor.

In another embodiment, a memory device is provided. The memory device includes an array of memory cells. Each memory cell includes an access transistor that is coupled to a trench capacitor. A first plate of the trench capacitor includes a micro-roughened surface of porous polysilicon. A second plate of the trench capacitor is disposed adjacent to the first plate. A number of bit lines are each selectively coupled to a number of the memory cells at a first source/drain region of the access transistor. A

number of word lines are disposed substantially orthogonal to the bit lines and are coupled to gates of a number of access transistors. A row decoder is coupled to the word lines and a column decoder is coupled to the bit lines so as to selectively access the cells of the array.

Brief Description of the Drawings

Figure 1 is a perspective view of an embodiment of a portion of an array of memory cells according to the teachings of the present invention.

Figures 2, 3, 4 and 5 are cross sectional views that illustrate an embodiment of a method for forming an array of memory cells according to the teachings of the present invention.

Figure 6 is a cross sectional view of another embodiment of a memory cell according to the teachings of the present invention.

Figure 7 is a block diagram of an embodiment of an electronic system and memory device according to the teachings of the present invention.

Detailed Description of the Invention

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific illustrative embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

In the following description, the terms wafer and substrate are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a

supporting semiconductor or insulating material, combinations of such layers, as well as other such structures that are known in the art.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizonal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

Figure 1 is a perspective view of an embodiment of a portion of an array of memory cells indicated generally at 100 and constructed according to the teachings of the present invention. Each memory cell is constructed in a similar manner. Thus, only memory cell 102D is described herein in detail. Memory cell 102D includes pillar 104 of single crystal semiconductor material. Pillar 104 is divided into first source/drain region 106, body region 108, and second source/drain region 110 to form access transistor 111. Pillar 104 extends vertically outward from substrate 101, for example, p-silicon. First source/drain region 106 and second source/drain region 110 each comprise, for example, heavily doped n-type single crystalline silicon (N+ silicon) and body region 108 comprises lightly doped p-type single crystalline silicon (P- silicon).

Word line 112 passes body region 108 of access transistor 111 in isolation trench 114. Word line 112 is separated from body region 108 of access transistor 104 by gate oxide 116 such that the portion of word line 112 adjacent to body region 108 operates as a gate for access transistor 111. Word line 112 may comprise, for example, N+ poly-silicon material that is deposited in isolation trench 114. Cell 102D is coupled in a column with cell 102A by bit line 118.

Memory cell 102D also includes storage capacitor 119 for storing data in the cell. A first plate of capacitor 119 for memory cell 102D is integral with second source/drain region 110 of access transistor 111. Thus, memory cell 102D may be more easily realizable when compared to conventional vertical transistors since there is no

need for a contact between second source/drain region 110 and capacitor 119. Surface 117 of second source/drain region 110 comprises a "micro-roughened" surface. This micro-roughened surface is formed by coating second source/drain region 110 with poly-silicon and treating the poly-silicon so as to form pores in surface 117. This increases the surface area of second source/drain region 110 and, thus, increases the capacitance of capacitor 119. The pores in surface 117 can be formed, for example, using the etching techniques described below.

Second plate 120 of capacitor 119 is common to all of the capacitors of array 100. Second plate 120 comprises a mesh or grid of n+ poly-silicon formed in deep trenches that surrounds at least a portion of second source/drain region 110 of each pillar 104A through 104D. Second plate 120 is grounded by contact with substrate 101 underneath the trenches. Second plate 120 is separated from source/drain region 110 by gate insulator 122.

Figures 2, 3, 4 and 5 are cross sectional views that illustrate an embodiment of a method for forming an array of memory cells according to the present invention. Figure 2 is a cross sectional view that shows a portion of an array of memory cells, indicated generally at 200. Array 200 includes pillars of semiconductor material 202 and 204 that are formed either outwardly from a bulk silicon wafer or outwardly from a silicon-on-insulator (SOI) structure. Pillar 202 includes first source/drain region 206, body region 208 and second source/drain region 210. As shown, first source/drain region 206 and second source/drain region 210 comprise heavily doped n-type semiconductor material and body region 208 comprises p-type semiconductor material. Pillar 204 is similarly constructed. Pillars 202 and 204 form the basis for vertical transistors used in array 200. It is noted that the conductivity types of the various regions of the pillars can be swapped so as to allow the formation of p-channel transistors.

The silicon pillar structure of a vertical transistor of array 200 may be formed using, for example, the techniques shown and described with respect to Figures 5A-5J of co-pending Application Serial No. 08/944,890, entitled "Circuit and Method for an Open Bit Line Memory Cell with A Vertical Transistor and Trench Plate Trench

Capacitor," filed on October 6, 1997 or with respect to Figures 5A-5M of Application Serial No. 08/939,742, entitled "Circuit and Method for a Folded Bit Line Memory Cell with Vertical Transistors and a Trench Capacitor," filed on October 6, 1997, which applications are incorporated herein by reference. Alternatively, the silicon pillars can be constructed to provide for a body contact for the transistors using techniques described with respect to Figures 5A-5P and 6A to 6O of co-pending, commonly assigned Application Serial No. 08/944,312, entitled "Circuit and Method for a Folded Bit Line Memory Using Trench Plate Capacitor Cells With Body Bias Contacts," filed on October 6, 1997 or with respect to Figures 5A-5O of Application Serial No. 08/939,732, entitled "Circuit and Method for an Open Bit Line Memory Cell With A Vertical Transistor and Trench Plate Trench Capacitor," filed on October 6, 1997, which applications are also incorporated herein by reference. Further, other conventional techniques for forming vertical transistors can also be used.

Once the basic silicon pillar structure is in place, surface 209 of first source/drain region 206 is roughened. Initially, nitride layer 212 (Si_3N_4) is deposited on silicon pillars 202 and 204. Optionally, nitride pad 213 is also deposited in trench 214 to protect the bottom of trench 214 during subsequent processing steps. For example, nitride pad 213 may be used when an SOI structure is used and the bottom of trench 214 is an insulator such as an oxide.

Trench 214 is filled with an oxide such that the entire structure of array 200 is covered. The oxide material outside of trench 214 is removed by, for example, chemical/mechanical polishing down to nitride layer 212. The oxide is further recessed into trench 214 to form oxide layer 216 as shown. Nitride masking layer 218 (Si_3N_4) is next deposited to protect body region 208 and second source drain region 210 during the formation of a micro-roughened surface. It is noted that masking layer 218 can be formed of any other material that can withstand a 6% aqueous solution of hydrofluoric acid (HF) or other etchant used to form a micro-roughened surface on first source/drain region 206.

As shown in Figure 3, nitride mask layer 218 is directionally etched to leave nitride mask layer 218 on selected surfaces of pillars 202 and 204. Oxide layer 216 is removed by, for example, an etching process. Amorphous silicon is deposited in trench 214 to form layer 220 with a thickness on the order of 10 to 40 nanometers (nm). The structure is heated to a sufficient temperature such that impurities diffuse out from first source/drain region 206 into layer 220. Thus, layer 220 becomes polysilicon that is doped to be the same conductivity type as first source/drain region 206. An etch that preferentially attacks intrinsic, undoped polysilicon is used to remove layer 220 from surfaces other than the surface of first source/drain region 206.

Surface 221 of layer 220 is next roughened to provide increased surface area for the trench capacitors of array 200. Surface 221 can be roughened in at least two different ways. First, layer 220 can be etched in a solution containing phosphoric acid (H_3PO_4). This forms micro-roughened surface 222 on polysilicon layer 220 in trench 214 as shown in Figure 4.

Alternatively, an anodic etch can be used to form the micro-roughened surface on layer 220. Figure 5 is a schematic diagram that illustrates an embodiment of a layout of equipment used to carry out the anodic etch. Bottom surface 246 of semiconductor wafer 201 is coupled to voltage source 234 by positive electrode 230. Further, negative electrode 232 is coupled to voltage source 234 and is placed in a bath of 6% aqueous solution of hydrofluoric acid (HF) on surface 245 of semiconductor wafer 201. It is noted that surface 245 includes layer 220 that is to be roughened by the anodic etch.

In this example, illumination equipment 236 is also included because the surface to be roughened is n-type semiconductor material. When p-type semiconductor material is used, the illumination equipment is not required. Illumination equipment 236 assures that there is a sufficient concentration of holes in layer 220 as required by the anodic etching process. Illumination equipment 236 includes lamp 238, IR filter 240, and lens 242. Illumination equipment 236 focuses light on surface 246 of semiconductor wafer 201.

In operation, layer 220 provides a high density of nucleation sites that are used by the anodic etch to roughen the surface of layer 220. Voltage source 234 is turned on and provides a voltage across positive and negative electrodes 230 and 232. Etching current flows from positive electrode 230 to surface 245 . This current forms pores in surface 221 of layer 220. Further, illumination equipment illuminates surface 246 of semiconductor wafer 201 so as to assure a sufficient concentration of holes for the anodic etching process. The anodic etching process produces a porous or roughened surface 222 on layer 220 as shown in Figure 4 such that the effective surface area of first source/drain region 206 is increased.

The size and shape of the pores in layer 220 depends on, for example, the anodization parameters such as HF concentration, current density, and light illumination. The spatial structure of the pores reflects the available paths for the etching current to flow from surface 245 to positive electrode 230. By adjusting the anodic etching parameters, the approximate diameter of the pores can be controlled with typically the smallest pore diameter on the order of 2 nanometers.

Array 200 is completed using, for example, the techniques described in the applications incorporated by reference above.

Figure 6 is a cross sectional view of another embodiment of a memory cell according to the teachings of the present invention. Memory cell 600 includes a conventional lateral transistor 602 with first source/drain region 604, body region 606 and second source/drain region 608. Transistor 602 also includes gate 610 that may be formed as part of a word line in a memory array as is known in the art. Bit line 612 is coupled to first source/drain region 604.

Memory cell 600 also includes trench capacitor 614. Substrate 616 forms a first plate of trench capacitor 614. Surface 618 of substrate 616 in trench 620 is formed with a micro-roughened surface using, for example, one of the techniques described above by depositing and etching a polysilicon layer in trench 620. Trench capacitor 614 also includes dielectric layer 622 that separates surface 618 from second plate 624. Second plate 624 comprises, for example, poly-silicon. Substrate 616 comprises single crystal

silicon. A layer of polysilicon material is deposited on a surface of the single crystal silicon of substrate 616 in forming micro-roughened surface 618. Second plate 624 of trench capacitor 614 is coupled to second source/drain region 608 by polysilicon strap 630.

In the example of Figure 6, transistor 602 comprises an n-channel transistor with heavily doped n-type source/drain regions and a body region formed in lightly doped p-type silicon well. Further, substrate 616 comprises a heavily doped p-type semiconductor substrate. Since substrate 616 comprises p-type material, the anodic etch, without illumination, can be used to form micro-roughened surface 618.

Memory cell 600 is included in an array of similar memory cells to store and retrieve data using conventional techniques.

Figure 7 is a block diagram of an illustrative embodiment of the present invention. This embodiment includes memory device 700 that is coupled to electronic system 702 by control lines 704, address lines 706 and input/output (I/O) lines 708. Electronic system 702 comprises, for example, a microprocessor, a processor based computer, microcontroller, memory controller, a chip set or other appropriate system for reading and writing data in a memory device. Memory device 700 includes array of memory cells 710 that is coupled to word line decoder 714 and sense amplifier 711. Array of memory cells 710 is constructed with memory cells that include trench capacitors with a micro-roughened surface that is formed using, for example, one of the techniques described above.

Word line decoder 714 includes word line drivers that are coupled to word lines of array 710. Sense amplifier 711 is coupled to bit line decoder 712. Bit line decoder 712 and word line decoder 714 are coupled to address lines 706. Bit line decoder 712 is coupled to I/O circuit 716. I/O circuit 716 is coupled to I/O lines 708. Control circuit 718 is coupled to control lines 704, sense amplifier 711, word line decoder 714, bit line decoder 712, and I/O circuit 716.

In operation, electronic system 702 provides signals on address lines 706 and control lines 704 when data is to be read from or written to a cell of array 710. Word

line decoder 714 determines the word line of a selected cell of array 710 using the address provided on address lines 706. Further, bit line decoder 712 determines the bit line of the selected cell of array 710. In a read operation, sense amplifier 711 detects the value stored in the selected cell based on bit lines of array 710. Sense amplifier 711 provides this voltage to I/O circuit 716 which, in turn, passes data to electronic system 702 over I/O lines 708. In a write operation, I/O circuit 716 passes data from I/O lines 708 to sense amplifier 711 for storage in the selected cell of array 710.

Conclusion

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, the techniques for forming roughened surfaces can be applied to p-type vertical transistors. In this case, when an anodic etch is used, no light source is needed to create the roughened texture on the surface of the p-type semiconductor material. Semiconductor materials other than silicon can be used. Further, the conductivity type of the semiconductor material can be altered without departing from the teachings of the present invention.

What is claimed is:

1. A method for forming a trench capacitor, the method comprising:

forming a trench in a semiconductor substrate;

depositing a conformal layer of semiconductor material in the trench;

roughening the surface of the conformal layer of semiconductor material;

forming an insulator layer outwardly from the roughened, conformal layer of semiconductor material; and

forming a polycrystalline semiconductor plate outwardly from the insulator layer in the trench.

2. The method of claim 1, wherein depositing a conformal layer of semiconductor material comprises depositing a layer of amorphous silicon and heating the amorphous silicon to form a polysilicon layer of the same conductivity type as the adjacent semiconductor substrate.

3. The method of claim 1, wherein roughening the surface of the conformal layer of semiconductor material comprises etching a surface of the semiconductor material with a phosphoric acid etch.

4. The method of claim 1, wherein roughening the surface of the conformal layer of semiconductor material comprises etching a surface of the semiconductor material with an anodic etch.

5. The method of claim 1, wherein roughening the surface of the conformal layer of semiconductor material comprises etching a surface of the semiconductor material with an anodic etch including illuminating the conformal layer of semiconductor material during the anodic etch.

6. The method of claim 1, wherein forming an insulator layer comprises growing an oxide layer outwardly from the roughened, conformal layer of semiconductor material.

7. A method for forming a memory cell with a trench capacitor, comprising:

forming a transistor including first and second source/drain regions, a body region and a gate in a layer of semiconductor material on a substrate;

forming a trench in the layer of semiconductor material;

depositing a conformal layer of semiconductor material in the trench;

roughening the surface of the conformal layer of semiconductor material;

forming an insulator layer outwardly from the roughened, conformal layer of semiconductor material;

forming a polycrystalline semiconductor plate outwardly from the insulator layer in the trench such that the polycrystalline semiconductor plate forms one of the plates of the trench capacitor; and

coupling the trench capacitor to one of the source/drain regions of the transistor.

8. The method of claim 7, wherein forming a transistor comprises forming a transistor with first and second source drain regions that are vertically aligned with the body region.

9. The method of claim 8, wherein coupling the trench capacitor to the first source/drain region comprises forming the trench for the trench capacitor adjacent to the first source/drain region.

10. The method of claim 7, wherein forming a transistor comprises forming a lateral transistor.

11. The method of claim 10, wherein coupling the trench capacitor to the first source/drain region comprises forming a strap from the polycrystalline semiconductor plate to the first source/drain region.

12. The method of claim 7, wherein depositing a conformal layer of semiconductor material comprises depositing a layer of amorphous silicon and heating the amorphous silicon to form a poly-silicon layer of the same conductivity type as the adjacent semiconductor substrate.

13. The method of claim 7, wherein roughening the surface of the conformal layer of semiconductor material comprises etching a surface of the semiconductor material with phosphoric acid.

14. The method of claim 7, wherein roughening the surface of the conformal layer of semiconductor material comprises performing an anodic etch of a surface of the semiconductor material.

15. The method of claim 7, wherein roughening the surface of the conformal layer of semiconductor material comprises performing an anodic etch of a surface of the semiconductor material while illuminating the semiconductor material.

16. The method of claim 7, wherein forming an insulator layer comprises growing an oxide layer outwardly from the roughened, conformal layer of semiconductor material.

17. A memory cell, comprising:

a lateral transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region;

a trench capacitor formed in a trench and coupled to the first source/drain region; and

wherein the trench capacitor includes a polycrystalline semiconductor plate formed in the trench that is coupled to the first source/drain region, a second plate formed by the substrate with a surface of the substrate in the trench roughened by etching a polycrystalline semiconductor material on the surface of the substrate, and an insulator layer that separates the polycrystalline semiconductor plate from the roughened surface of the substrate.

18. The memory cell of claim 17, wherein the polycrystalline semiconductor plate comprises polysilicon.

19. The memory cell of claim 17, wherein the second plate comprises a heavily doped p-type silicon substrate.

20. The memory cell of claim 17, wherein the second plate of the trench capacitor comprises the substrate with a surface in the trench that is roughened by an anodic etch.

21. The memory cell of claim 17, wherein the second plate of the trench capacitor comprises the substrate with a surface in the trench that is roughened by a phosphoric etch.

22. A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned;

wherein a surface of the first source/drain region is roughened by etching a polycrystalline semiconductor material on a surface of the first source/drain region; and

a trench capacitor with a plate that is formed in a trench that surrounds the roughened surface of the first source/drain region of the transistor.

23. The memory cell of claim 22, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon is roughened by etching the surface of the polysilicon with phosphoric acid.

24. The memory cell of claim 22, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon is roughened by etching the surface of the polysilicon with an anodic etch.

25. The memory cell of claim 22, wherein the polycrystalline semiconductor plate comprises polysilicon.

26. A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor includes a micro-roughened surface of porous polysilicon and a second plate of the trench capacitor is disposed adjacent to the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

27. The memory device of claim 26, wherein the first plate comprises a single crystalline silicon source/drain region of a vertical transistor with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon is roughened by etching the surface of the polysilicon with phosphoric acid.

28. The memory device of claim 26, wherein the first plate comprises a single crystalline silicon source/drain region of a vertical transistor with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon is roughened by etching the surface of the polysilicon with an anodic etch.

29. The memory device of claim 26, wherein the polycrystalline semiconductor plate comprises polysilicon.

30. The memory device of claim 29, wherein the access transistor comprises a lateral transistor that is coupled to the second plate of the trench capacitor.

Abstract of the Disclosure

A method for forming a trench capacitor. The method includes forming a trench in a semiconductor substrate. A conformal layer of semiconductor material is deposited in the trench. The surface of the conformal layer of semiconductor material is roughened. An insulator layer is formed outwardly from the roughened, conformal layer of semiconductor material. A polycrystalline semiconductor plate is formed outwardly from the insulator layer in the trench.

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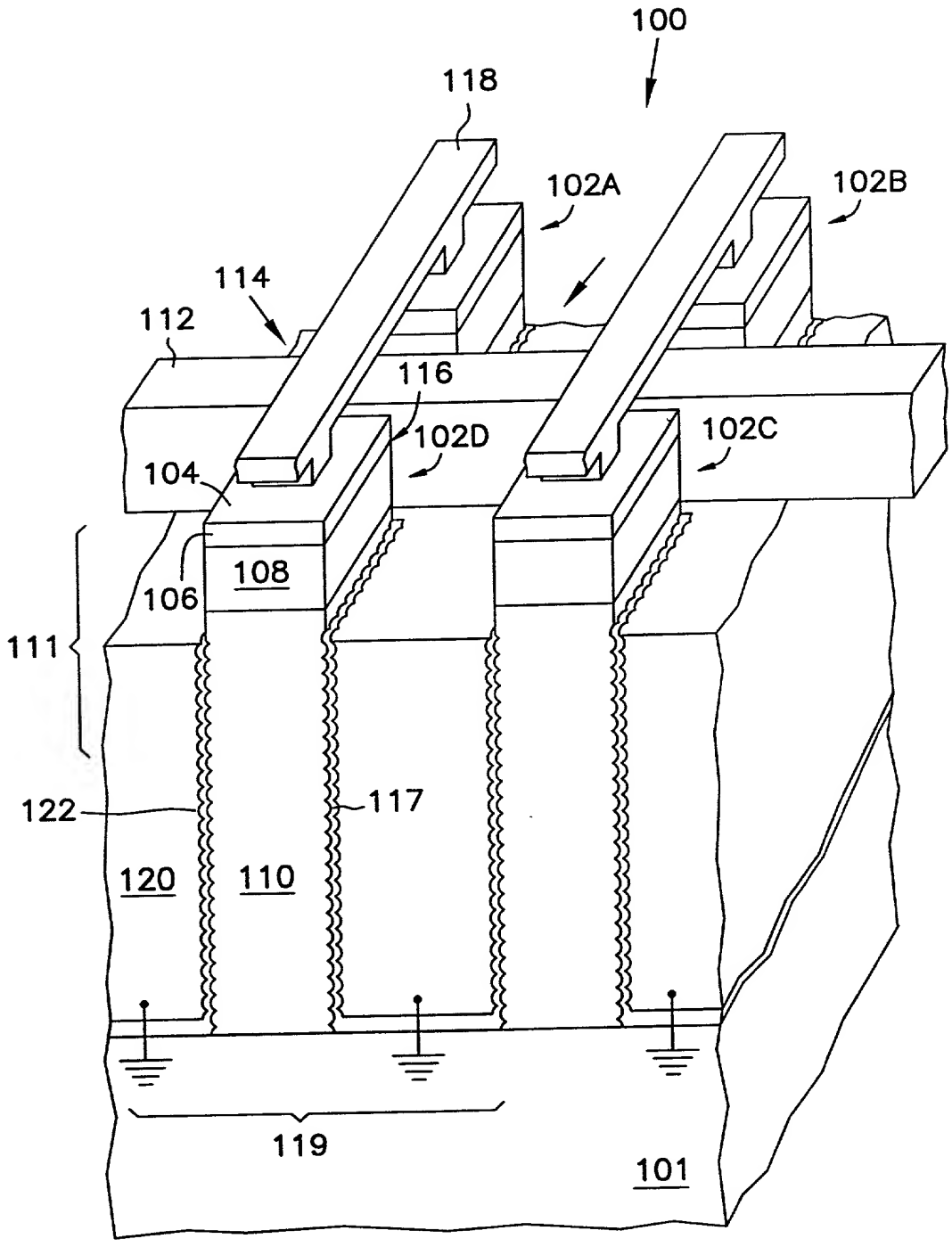
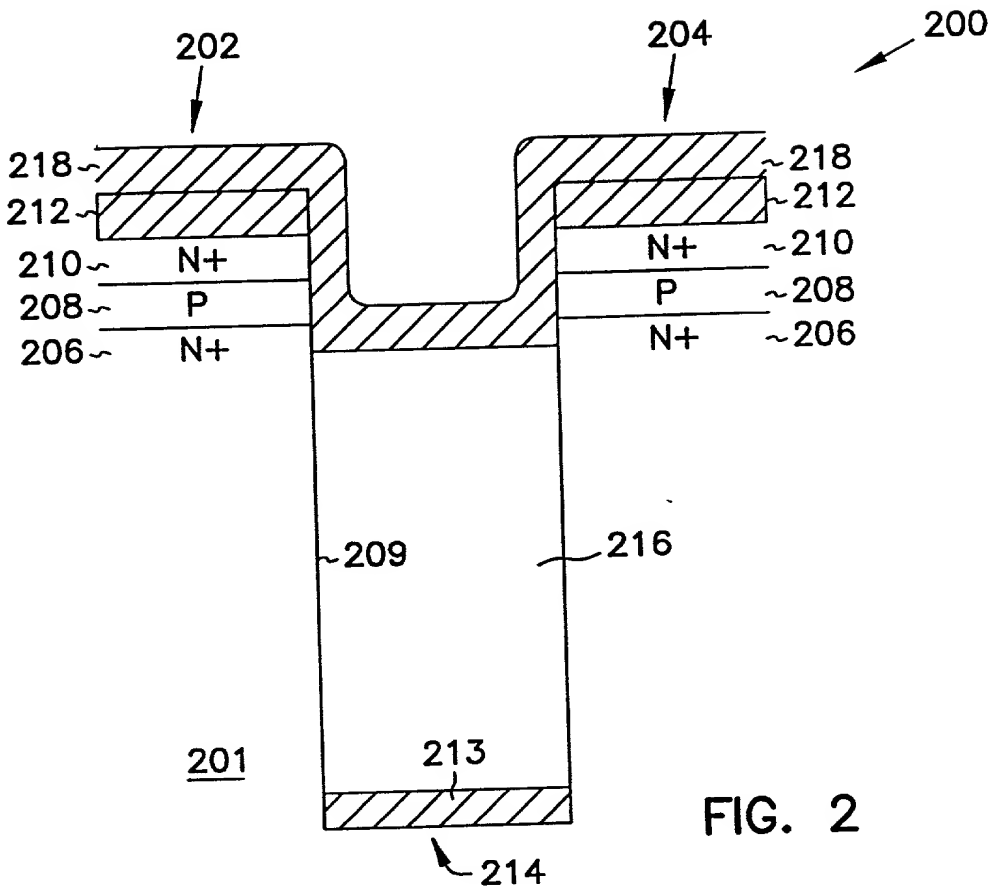

100
118
102A
102B
114
112
116
102D
102C
104
108
106
111
122
117
120
110
119
101

FIG. 1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202
204
218
212
210
N+
208
P
206
N+
218
212
N+
210
P
208
N+
206
209
216
201
213
214

FIG. 2

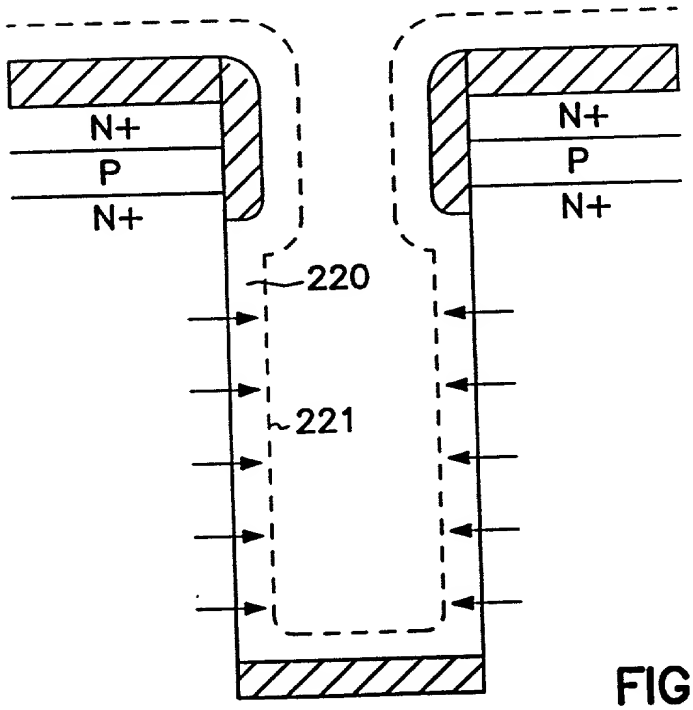
N+
P
N+
N+
P
N+
220
221

FIG. 3

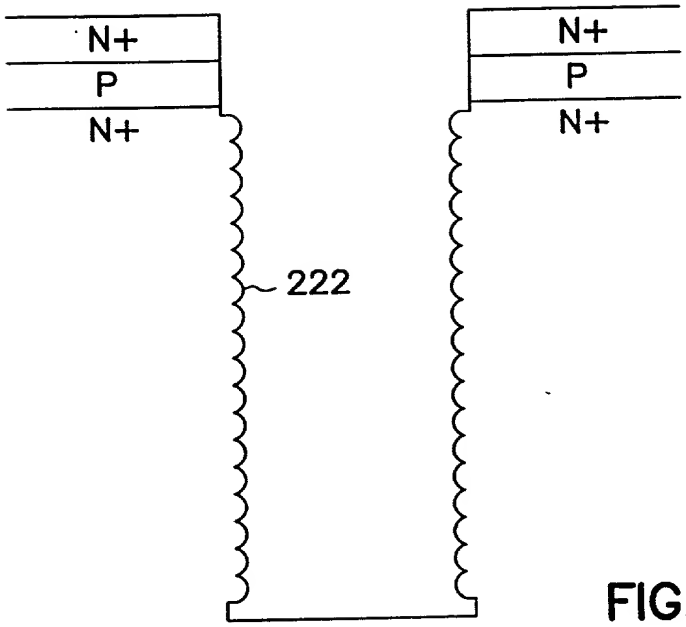
N+
P
N+
N+
P
N+
222

FIG. 4

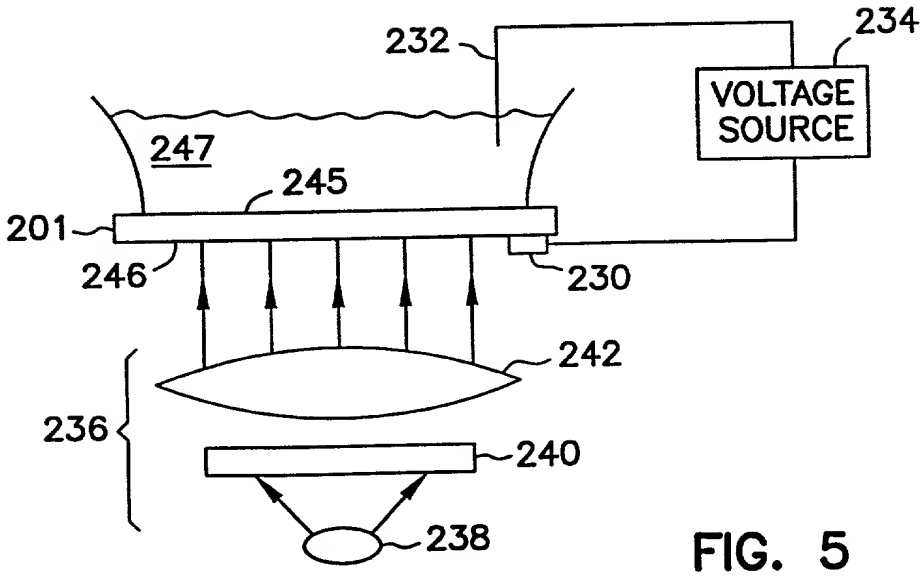
232
234
VOLTAGE SOURCE
247
245
201
246
230
242
236
240
238

FIG. 5

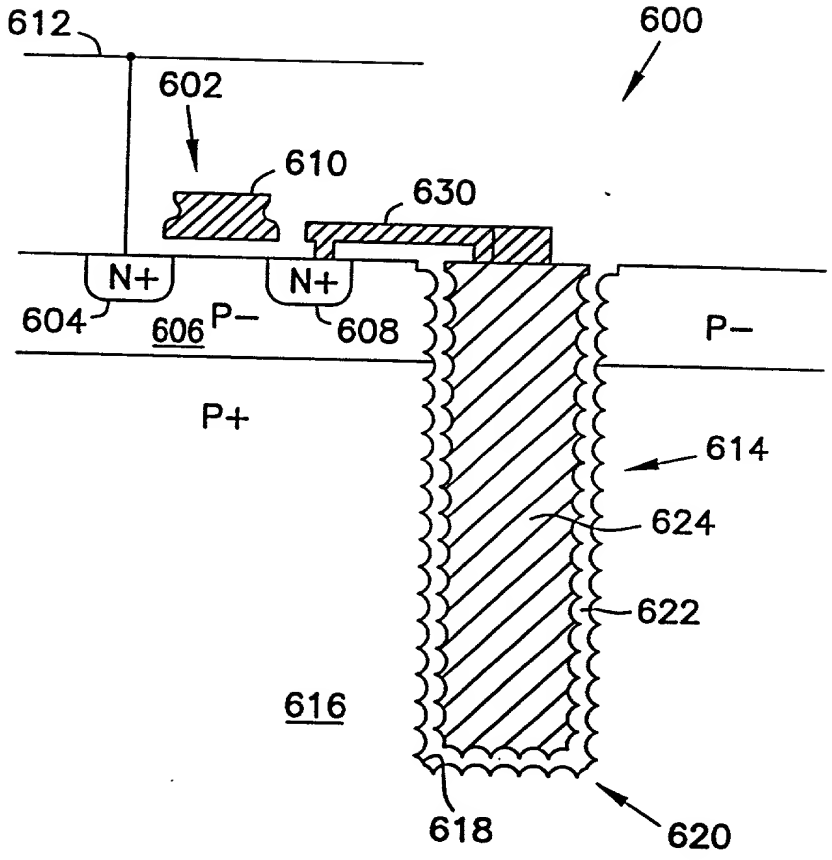

FIG. 6

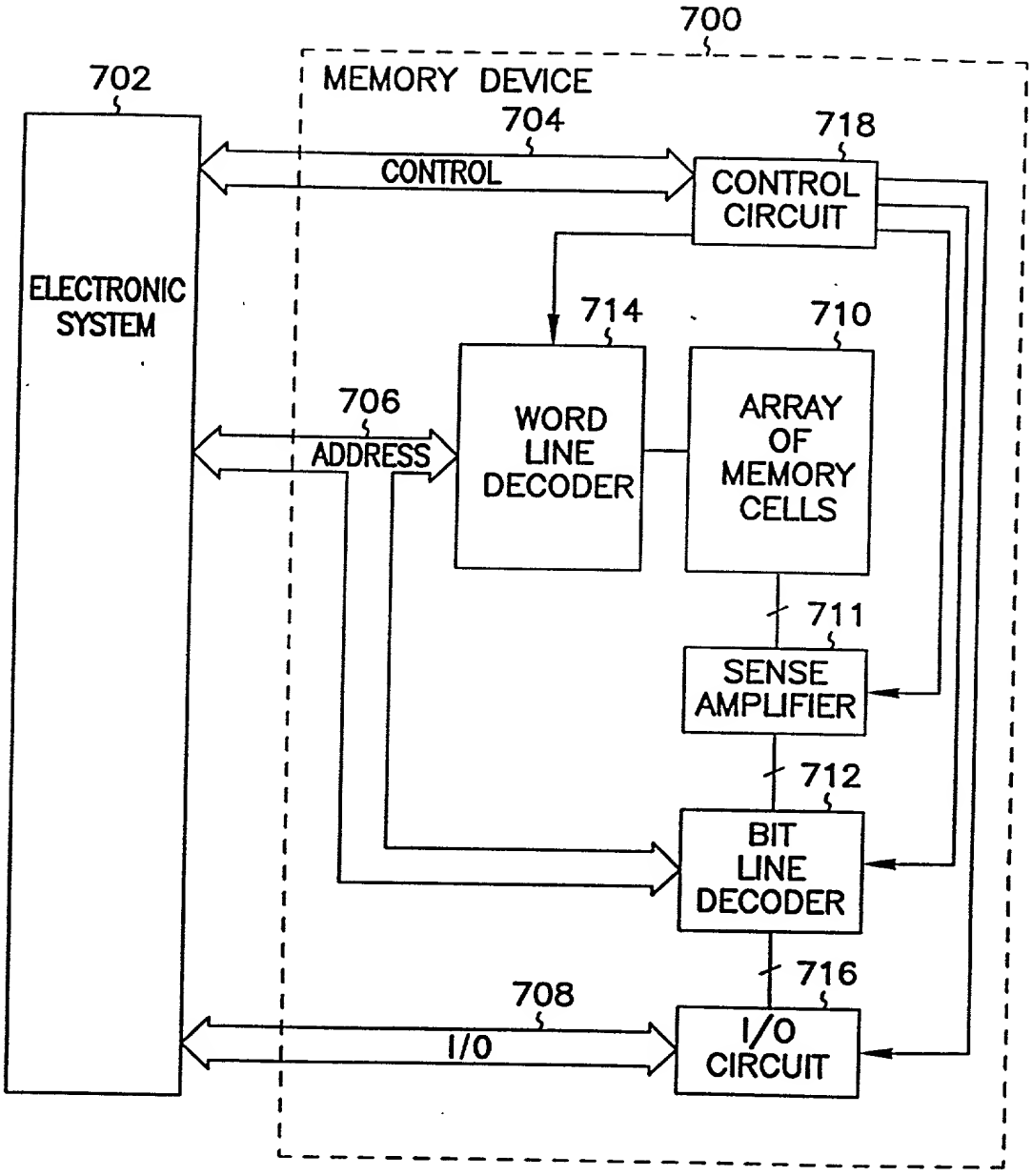
700
MEMORY DEVICE
702
ELECTRONIC SYSTEM
704
CONTROL
718
CONTROL CIRCUIT
714
710
706
ADDRESS
WORD LINE DECODER
ARRAY OF MEMORY CELLS
711
SENSE AMPLIFIER
712
BIT LINE DECODER
716
708
I/O
I/O CIRCUIT

FIG. 7

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

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I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought or the invention entitled: **CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED SEMICONDUCTOR SURFACES AND METHODS FOR FORMING THE SAME** .

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Brennan, Thomas F.	Reg. No. 35,075	Hofmann, Rudolph P., Jr.	Reg. No. 38,187	Schwegman, Micheal L.	Reg. No. 25,816
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Drake, Eduardo E.	Reg. No. 40,594	Kluth, Daniel J.	Reg. No. 32,146	Viksnins, Ann S.	Reg. No. 37,748
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Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: 30 DEC 97
Leonard Forbes

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Citizenship: **United States of America** Residence: **Berkeley Heights, NJ**
Post Office Address: 261 Lorraine Drive
Berkeley Heights, NJ 07922

Signature: _____ Date: _____
Joseph E. Geusic

Full Name of joint inventor number 3 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: _____ Date: _____
Kie Y. Ahn

Full Name of inventor:
Citizenship: Residence:
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Signature: _____ Date: _____

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(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associat with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

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Post Office Address: 965 NW Highland Terrace
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Signature: _____ Date: _____
Leonard Forbes

Full Name of joint inventor number 2 : **Joseph E. Geusic**
Citizenship: **United States of America** Residence: **Berkeley Heights, NJ**
Post Office Address: 261 Lorraine Drive
Berkeley Heights, NJ 07922

Signature: Joseph E. Geusic Date: 1/15/98
Joseph E. Geusic

Full Name of joint inventor number 3 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: _____ Date: _____
Kie Y. Ahn

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Citizenship: Residence:
Post Office Address:

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: Kie Y. Ahn Date: Dec. 26, 1997
Kie Y. Ahn

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Citizenship: Residence:
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(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associ with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.